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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/756,393	01/14/2004	Ji-Yong Park	6161.0109.US	1886

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EXAMINER	
WILSON, SCOTT R	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/756,393	PARK ET AL.	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-6, 8-10 and 12-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.. As to claim 1, Yamaguchi et al., Figures 6 discloses a CMOS thin film transistor, comprising: an active channel (3) of a P-type thin film transistor, the active channel being formed in polycrystalline silicon, and in Figure 5, an active channel (3) of a N- type thin film transistor, the active channel being formed in polycrystalline silicon, primary grain boundaries in the P-type thin film transistor (4), primary grain boundaries in the N-type thin film transistor (4), wherein a direction of the active channel of the P-type transistor is different from a direction of the active channel of the N-type transistor such that the primary grain boundaries of the P-type thin film transistor are at an angle of about 60° to about 120° with respect to the active channel direction of the P-type thin film transistor and the primary grain boundaries of the N- type thin film transistor are out an angle of about -30° to about 30° with respect to the active channel direction of the N-type thin film transistor.

As to claim 2, Yamaguchi et al. discloses that the p-type transistor is formed with low current mobility and that the n-type transistor is formed with high current mobility (paragraph 0035, right-hand column, lines 12-15).

As to claim 3, Yamaguchi et al. discloses that the p-type transistor is formed with low threshold voltage and that the n-type transistor is formed with high threshold voltage (paragraph 0049, page 6, left-hand column, lines 9-17).

As to claim 4, Yamaguchi et al. discloses that the p-type transistor is formed with low threshold voltage and that the n-type transistor is formed with high threshold voltage, with reduced difference in threshold voltage (paragraph 0049, page 6, left-hand column, lines 20-23).

As to claim 5, Yamaguchi et al. discloses that the p-type transistor is formed with low threshold voltage and that the n-type transistor is formed with high threshold voltage, with reduced difference in threshold voltage (paragraph 0049, page 6, left-hand column, lines 20-23).

As to claim 6, Yamaguchi et al., Figures 5 and 6, discloses that the length of the channel in the p-type and n-type transistors are substantially equal.

As to claim 8, Yamaguchi et al., Figure 6, discloses that the primary grain boundaries of the p-type transistor are substantially perpendicular to the active channel direction, and Figure 5 discloses that the primary grain boundaries of the n-type transistor are substantially horizontal to the active channel direction.

As to claim 9, Yamaguchi et al., Figure 6, discloses that the primary grain boundaries of the p-type transistor are perpendicular to the active channel direction, and Figure 5 discloses that the primary grain boundaries of the n-type transistor are horizontal to the active channel direction.

As to claim 10, Yamaguchi et al., Figure 6, discloses that the majority of primary grain boundaries of the p-type transistor are substantially perpendicular to the active channel direction, and Figure 5 discloses that the majority of primary grain boundaries of the n-type transistor are substantially horizontal to the active channel direction.

Claims 12 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.. As to claim 12, Yamaguchi et al., Figures 6 discloses a CMOS thin film transistor, comprising: an active channel (3) of a P-type thin film transistor, the active channel being formed in polycrystalline silicon, and in Figure 5, an active channel (3) of a N- type thin film transistor, the active channel being formed in polycrystalline silicon, primary grain boundaries in the P-type thin film transistor (4), primary grain

boundaries in the N-type thin film transistor (4), wherein a direction of the active channel of the P-type transistor is different from a direction of the active channel of the N-type transistor such that the primary grain boundaries of the P-type thin film transistor are at an angle of about 60° to about 120° with respect to the active channel direction of the P-type thin film transistor and the primary grain boundaries of the N-type thin film transistor are out an angle of about -30° to about 30° with respect to the active channel direction of the N-type thin film transistor. Yamaguchi et al. further discloses (Abstract) that the transistor comprises a display device.

As to claim 13, Yamaguchi et al. discloses (paragraph 0059) that the display device can be a liquid crystal display device.

Claims 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi et al.. As to claim 14, Yamaguchi et al., Figures 6 discloses a CMOS thin film transistor, comprising: an active channel (3) of a P-type thin film transistor, the active channel being formed in polycrystalline silicon, and in Figure 5, an active channel (3) of a N- type thin film transistor, the active channel being formed in polycrystalline silicon, primary grain boundaries in the P-type thin film transistor (4), primary grain boundaries in the N-type thin film transistor (4), wherein a direction of the active channel of the P-type transistor is different from a direction of the active channel of the N-type transistor such that the primary grain boundaries of the P-type thin film transistor are at an angle of about 60° to about 120° with respect to the active channel direction of the P-type thin film transistor and the primary grain boundaries of the N-type thin film transistor are out an angle of about -30° to about 30° with respect to the active channel direction of the N-type thin film transistor. Yamaguchi et al. further discloses (Abstract) that the amorphous silicon is crystallized using a laser.

As to claim 15, Yamaguchi et al. discloses that the angle between the grain boundaries of the N-type thin film transistor and the active channel of the N-type thin film transistor is substantially equal to zero and the angle between the grain boundaries of the P-type thin film transistor and the active channel of the P-type thin film transistor is substantially equal to 90°.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Kasahara et al.. Yamaguchi et al. discloses the invention of claim 1, as described above. Yamaguchi et al. does not disclose expressly the polysilicon formed by a sequential lateral solidification (SLS) method. Kasahara et al., (col. 3, lines 37-41) discloses crystallization using the SLS method. At the time of invention, it would have been obvious to a person of ordinary skill in the art to use the SLS method for crystallization. The motivation for doing so would have been to realize super lateral growth at an arbitrary location (Kasahara et al, col. 3, lines 40-41). Therefore, it would have been obvious to combine Kasahara et al. with Yamaguchi et al. to obtain the invention as specified in claim 7.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Ohtani. Yamaguchi et al. discloses the invention of claim 1, as described above. Yamaguchi et al. does not disclose expressly a LDD structure formed in either transistor. Ohtani, (col. 11, line 21) discloses an LDD structure formed in a transistor with grain boundaries in an amorphous silicon layer (Abstract). At the time of invention, it would have been obvious to a person of ordinary skill in the art to form an LDD structure in the transistor of Yamaguchi et al.. The motivation for doing so would have been to reduce the OFF current of the transistor (Ohtani, col.; 11, line 19). Therefore, it would have been obvious to combine Ohtani with Yamaguchi et al. to obtain the invention as specified in claim 11.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 571-272-1925. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

srw
August 20, 2004

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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